AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. – 6. (Cancelled)

7. (Previously Presented) A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

a first outputting section for performing NANDing arithmetic between the output of said first inversion section and a second input signal and outputting a first resulting signal; and

a second outputting section for performing NANDing arithmetic between the output of said second inversion section and an inverted signal of the second input signal and outputting a second resulting signal;

said first outputting section and said second outputting section being switched with the second input signal and the inverted signal of the second input signal, said first outputting section outputs the first resulting signal and said second outputting section outputs the second resulting signal.

8. (Currently Amended) ~~The~~ A logic circuit ~~as claimed in claim 1, further,~~ comprising:

a first inversion section for inverting a first input signal having a first logic level and outputting an inverted first input signal;

a second inversion section for inverting a second input signal having a logic level always being opposite to the first logic level, and outputting an inverted second input signal;

a transmission section for receiving the inverted first input signal and the inverted second input signal and outputting one of the inverted first input signal and the inverted second input signal;

a first switching section provided on an input side of said first inversion section and performing switching of whether the first input signal is passed to the first inversion section or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and performing switching of whether the second input signal is passed to the second inversion section or blocked in accordance with the external control signal,

wherein the transmission section comprises electrically connected transistors that respectively receive the inverted first input signal and the inverted second input signal, and the connected transistors select between outputting the inverted first input signal and the inverted second input signal in response to only an externally controllable selection signal and an inverted signal of the selection signal.

9. – 17. (Cancelled)

18. (Currently Amended) ~~The~~ A logic circuit ~~as claimed in claim 17, further,~~ comprising:

a first inversion section for inverting a first input signal with a first logic level and outputting the inverted first input signal;

a second inversion section for inverting a second input signal with a second logic level, which is always an opposite logic level to the first logic level, and outputting the inverted second input signal; and

a transmission section for receiving the inverted first input signal and the inverted second input signal and outputting either the inverted first input signal or the inverted second input signal;

a first switching section provided on an input side of said first inversion section and performing switching of whether the first input signal is passed to the first inversion section or blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and performing switching of whether the second input signal is passed to the second inversion section or blocked in accordance with the external control signal.